LEVEL III

(1)

CALIFORNIA INSTITUTE OF TECHNOLOGY

PASADENA, CALIFORNIA 91125

ITER SCIENCE 256-80

(9) Research and development ~~RED~~ STATUS REPORT, 1 Dec 80-1 Mar 81,

ARPA ORDER NO. 3771 Amend. No. 1

CONTRACTOR: Caltech

(15) CONTRACT NUMBER: ~~N00014-79-C-0924~~, ARPA Order-3771

EFFECTIVE DATE OF CONTRACT: September 1, 1979

EXPIRATION DATE OF CONTRACT: August 31, 1981

(10) PRINCIPAL INVESTIGATOR: Carver/Mead

TELEPHONE NUMBER: (213) 356-6811

(16) SHORT TITLE: Demonstration of the Use of VLSI Design Rules, Standards, and Interfaces.

REPORTING PERIOD: December 1, 1980 to March 1, 1981

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DESCRIPTION OF PROGRESS

Progress is reported for each element of Tasks 1, 2 and 3.

TASK 1

1. Consultation from Fabrication Lines

Work completed; no further progress to report.

2. CMOS-SOS and NMOS-Si Gate Test-Chips

Further evaluation of the NMOS test-chip results from the MPC runs has led to further modification of the NMOS test-chip. This modified design has been submitted to ISI (the Information Sciences Institute of U.S.C.) for use in future MPC runs.

In addition, NBS requested the inclusion of a number of test-structures of their own design on the SOS test-chips. These were incorporated into the SOSTWO test-chip design.

3. Geometrical Design Rules

No new progress to report.

4. Speed and Timing Rules

The final report is in the process of being revised (see last quarterly report).

5. CIF

A modification of the standard CIF 2.0, SOSCIF, was completed at this time to generate the additional two mask layers required by CMOS-SOS. This version of CIF is of use primarily in the design of test-structures such as four-terminal transistors. It differs from the standard CIF 2.0 in specifying seven explicit CIF layers instead of six.

6. Testability Rules

Work is proceeding - see last quarterly report.

TASK 2

1. Design-Rule Checker

Deleted (see last quarterly report).

2. CIF/APPLICON, CALMA Conversion Software

The CIF to APPLICON software development has been completed.

3. Circuit Design

Work completed; no progress to report.

TASK 3

1. Contract Negotiations

Informal agreements were reached with Hughes and Rockwell for CMOS-SOS fabrication. JPL will supply the mask set which will be generated through ISI by Micromask.

2. Fabrication

Hughes has verified that Caltech design assumptions are compatible with their fabrication line. They have supplied mask-design information regarding required layers, and the CALMA format tapes for generating auto alignment targets and the Hughes test chips.

CHANGES IN KEY PERSONNEL: none

SUMMARY OF SUBSTANTIVE INFORMATION DERIVED FROM SPECIAL EVENTS: none

PROBLEMS ENCOUNTERED OR ANTICIPATED: none

ACTION REQUIRED BY THE GOVERNMENT:

The contract extension to August 31, 1981 has been received; no further action is required.

FISCAL STATUS:

1.	Amount currently on contract:		$630,718
2.	Expenditures and commitments to date:		
	Campus Salaries and Contracts:	56,643	
	JPL Salaries and Contracts:	494,323	
			$550,966
3.	Funds required to complete all Tasks:		$79,752

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